

Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application:

Claims 9-15 are withdrawn.

18. (Original) A transistor, comprising:
a single crystal substrate having a lattice constant;
a channel layer disposed over the substrate, the channel layer having a lattice constant different from the lattice constant of the substrate;
a Schottky layer disposed over the channel layer, the Schottky layer having a lattice constant different from the lattice constant of the substrate;
a resistive layer disposed over the Schottky layer; and
a contact layer disposed over the resistive layer, the contact layer having a first recess therein, such first recess having a bottom surface terminating in a top surface of the resistive layer;
a second recess having sidewalls in the resistive layer and the Schottky layer, such second recess having a bottom surface terminating in the Schottky layer.

19. (Original) The transistor recited in claim 18 wherein the lattice constant of the Schottky layer and a thickness of the Schottky layer are selected to compensate for differences in strain between: (a) the channel layer and the substrate; and, (b) the Schottky layer and the substrate.

20. (Original) The transistor recited in claim 19 wherein the lattice constant of the Schottky layer is smaller than the lattice constant of the substrate and the lattice constant of the channel layer is larger than the lattice constant of the substrate.

21. (Original) The transistor recited in claim 20 wherein the lattice constant of the substrate is intermediate the lattice constant of the channel layer and the lattice constant of the Schottky

layer, the difference in lattice constants resulting in a compressive strain on the channel layer and a tensile strain on the Schottky layer.

22. (Original) The transistor recited in claim 18 wherein the Schottky layer has an indium concentration and the indium concentration in the Schottky layer is lower than an indium concentration in the channel layer.

23. (Original) The transistor recited in claim 22 wherein the substrate comprises indium phosphide.

24. (Original) The transistor recited in claim 22 wherein the Schottky layer comprises approximately $\text{Al}_{0.60}\text{In}_{0.40}\text{As}$.

25. (Original) The transistor recited in claim 22 wherein the channel layer comprises approximately $\text{Ga}_{0.35}\text{In}_{0.65}\text{As}$.

26. (Original) The transistor recited in claim 23 wherein the Schottky layer comprises approximately $\text{Al}_{0.60}\text{In}_{0.40}\text{As}$ and the channel layer comprises approximately $\text{Ga}_{0.35}\text{In}_{0.65}\text{As}$.

27. (Original) A transistor, comprising;
a substrate having a lattice constant;
a channel layer disposed over the substrate, the channel layer having a lattice constant;
a Schottky layer disposed over the channel layer, the Schottky layer having a lattice constant;
a resistive layer disposed over the Schottky layer; and
a contact layer disposed over the resistive layer, the contact layer having a first recess therein, such first recess having a bottom surface terminating in a top surface of the resistive layer; and
a second recess having sidewalls in the resistive layer and the Schottky layer, such second recess having a bottom surface terminating in the Schottky layer;

wherein at least one of the channel and Schottky layers has an indium concentration such that at least one of the lattice constants of the channel layer and lattice constant of the Schottky layer is different from the lattice constant of the substrate and a difference between conduction band levels of the channel and Schottky layers is larger than if the channel and Schottky layers had the same lattice constant as the substrate.

28. (Original) The transistor recited in claim 27 wherein the larger conduction band discontinuity occurs between the Schottky and channel layers.

29. (Original) The transistor recited in claim 27 wherein the Schottky layer comprises approximately $\text{Al}_{0.60}\text{In}_{0.40}\text{As}$ and the channel layer comprises approximately $\text{Ga}_{0.35}\text{In}_{0.65}\text{As}$.

30. (Original) The transistor recited in claim 25 wherein the channel layer has an indium concentration such that the channel layer can support larger currents than if the channel layer and the substrate had the same lattice constant.

31. (Cancelled)

32. (Cancelled)

33. (Currently amended) ~~The transistor recited in claim 32~~ A transistor, comprising:

- a semi-insulating indium phosphide substrate;
- a channel layer of $\text{Ga}_x\text{In}_{1-x}\text{As}$ disposed over the substrate layer;
- a Schottky layer of $\text{Al}_y\text{In}_{1-y}\text{As}$ disposed over the channel layer;
- a resistive layer disposed over the Schottky layer;
- a contact layer disposed over the resistive layer, the contact layer having a first recess,
- and the resistive layer and the Schottky layer having a second recess;
- a source electrode in ohmic contact with the contact layer;
- a drain electrode in ohmic contact with the contact layer; and
- a gate electrode in Schottky contact with the Schottky layer

further comprising a first doped layer, and a second doped layer; and
further comprising a ratio of silicon doping concentration approximately 2.5 to 1.5
between the first doped layer and the second doped layer.

34. (Currently amended) ~~The transistor recited in claim 32~~ A transistor, comprising:

a semi-insulating indium phosphide substrate;
a channel layer of $\text{Ga}_x\text{In}_{1-x}\text{As}$ disposed over the substrate layer;
a Schottky layer of $\text{Al}_y\text{In}_{1-y}\text{As}$ disposed over the channel layer;
a resistive layer disposed over the Schottky layer;
a contact layer disposed over the resistive layer, the contact layer having a first recess,
and the resistive layer and the Schottky layer having a second recess;
a source electrode in ohmic contact with the contact layer;
a drain electrode in ohmic contact with the contact layer; and
a gate electrode in Schottky contact with the Schottky layer;
further comprising a first doped layer, and a second doped layer; and

wherein the resistive layer further comprises approximately $\text{Al}_{0.48}\text{In}_{0.52}\text{As}$ and the contact layer
further comprises approximately $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$.